W-Band CPW RF MEMS Circuits on Quartz Substrates

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***Abstract*—This paper presents W-band coplanar waveguide RF microelectromechanical system (MEMS) capacitive shunt switches with very low insertion loss (-0.2 to -0.5 dB) and high-isolation (≤ -30 dB) over the entire W-band frequency range. It is shown that full-wave electromagnetic modeling using *Sonnet* can predict the performance of RF MEMS switches up to 120 GHz. Also presented are W-band 0°/90° and 0°/180° switched-line phase shifters with very good insertion loss (1.75 dB/bit at 90 GHz) and a wide bandwidth of operation (75–100 GHz). These circuits are the first demonstration of RF MEMS digital-type phase shifters at W-band frequencies and they outperform their solid-state counterparts by a large margin.**

***Index Terms*—Microelectromechanical system (MEMS), microwave, millimeter wave, phase shifters, switches.**

I. Introduction

SHUNT AND series RF microelectromechanical system (MEMS) switches have been demonstrated from 1 to 120 GHz [1]–[10]. While series switches are mainly used from dc–40 GHz, capacitive shunt switches are better suited for 10–120-GHz applications. This paper presents W-band coplanar waveguide (CPW) capacitive shunt switches on quartz substrates in a T-match and a π-match configuration with very low insertion loss (-0.2 to -0.5 dB) and excellent isolation response (≤ -30 dB). Both designs result in excellent performance over the entire W-band range. The insertion loss of the MEMS circuits is around 1 dB better than state-of-the-art p-i-n diode switches at W-band frequencies [11], [12]. The switches are then used to build 1-bit 0°/90° and 0°/180° W-band phase shifters.

MEMS phase shifters have been already demonstrated at 6–60-GHz frequencies in both digital and analog implementations [13]–[18]. The phase shifters presented in this paper are switched-line designs in a CPW configuration and result in wide-band performance almost over the entire W-band region with a very low insertion loss.

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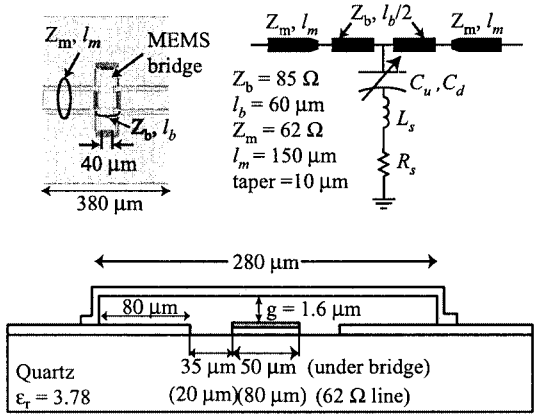


Fig. 1. CPW shunt capacitive MEMS switch and its equivalent circuit.

II. W-Band MEMS Switches

A. T-Match Design

Fig. 1 shows a W-band CPW shunt capacitive MEMS switch on a quartz substrate and its equivalent circuit model. The switch is 40-μm wide, 280-μm long, 8000-Å thick, and is suspended 1.5–1.6 μm above the central conductor. The switch is inserted in a 62-Ω CPW t-line with dimensions of $\mathrm{G/W/G} = 20/80/20$ μm, but the line is tapered underneath the bridge to $\mathrm{G/W/G} = 35/50/35$ μm so as to result in a lower up-state capacitance. For a 40×50 $\mu\mathrm{m}^2$ pull-down electrode, the parallel plate up-state capacitance is $C_{\mathrm{upp}} = \epsilon_o A/g = 11$ fF and the total up-state capacitance is around 14 fF (30% fringing capacitance). The Si_3N_4 dielectric thickness underneath the MEMS bridge is 1500 Å, resulting in a maximum down-state capacitance of 900 fF. In general, due to the dielectric roughness, the down-state capacitance is around 400 fF. The substrate thickness is not critical for the CPW designs and both 150- and 500-μm-thick substrates were used. The MEMS switch fabrication follows the well-established procedure in [8]. The switches are biased through W-band probe bias tees and have a pull-down voltage of $V_p = 40$ V. The corresponding spring constant is 22 N/m and the mechanical resonance frequency is around 103 kHz. The residual stress is estimated to be around $\sigma = 75$ MPa [19]. For an actuation voltage of $V_s = 55$ V, the switching time is 4 μs as follows [19]:

$$t_s = \frac{V_p}{\omega_o V_s}\sqrt{\frac{27}{2}} \tag{1}$$

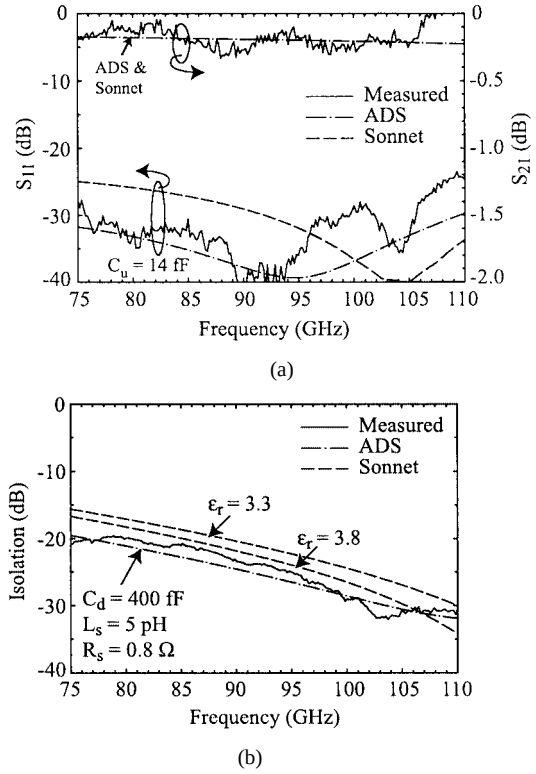


Fig. 2. Measured S-parameters of a T-match switch: (a) in the up-state position and (b) in the down-state position.

Fig. 2 presents the measurements for a single CPW MEMS capacitive switch. The high-impedance lines (62 Ω) on either side of the bridge along with the small section underneath the bridge are equivalent to a series inductance and constitute a T-match circuit [20]. The measured return loss is better than −25 dB over the whole W-band range and fits an up-state capacitance $C_u = 14 \pm 1$ fF. The measured insertion loss is around −0.2 dB and the reference planes are 380 μm apart. *ADS*[1] and full-wave *Sonnet*[2] simulations fit the measured results very well. They accurately predict the insertion loss when the metal conductivity in *ADS* and *Sonnet* is changed to match the measured 62-Ω CPW reference t-line loss of 4 dB/cm at 90 GHz.

In the down-state position, the MEMS bridge has a measured isolation better than −20 dB from 75 to 110 GHz and better than −30 dB above 100 GHz [see Fig. 2(b)]. The fitted CLR model using *ADS* is $C_d = 400 - 450$ fF, $L_s = 4 - 5$ pH and $R_s = 0.8 - 1\ \Omega$ and the C_d/C_u ratio is 30. It is estimated that these values are accurate to within 10% due to the calibration accuracy at the W-band. The difference between the fitted down-state capacitance (400–450 fF) and the calculated parallel-plate capacitance (900 fF) is due to the surface roughness between the bridge membrane and the silicon–nitride layer. Actually, the decrease in the down-state capacitance is beneficial at the W-band since it increases the down-state LC resonance frequency to 105 GHz. In fact, the isolation of a capacitive shunt switch is given by

$$|S_{21}|^2 \simeq \begin{cases} \dfrac{4}{\omega^2 C_d^2 Z_o^2}, & \text{for } f \ll f_{\text{res}} \\ \dfrac{4R_s^2}{Z_o^2}, & \text{for } f = f_{\text{res}} \\ \dfrac{4\omega^2 L^2}{Z_o^2}, & \text{for } f \gg f_{\text{res}} \end{cases} \tag{2}$$

with the down-state resonant frequency being

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{C_d L_s}} \tag{3}$$

and the maximum isolation is given at the resonance frequency by the value of the bridge series resistance ($R_s = 0.8 - 1\ \Omega$ at 100 GHz). In the *Sonnet* simulations, the decrease in the down-state capacitance is taken into account by decreasing the dielectric constant of the silicon–nitride brick from 7.6 to 3.8 ($C_d = 450$ fF) and 3.3 ($C_d = 400$ fF). The dielectric roughness was not characterized experimentally for these particular circuits, but a thorough analysis was done earlier at The University of Michigan at Ann Arbor and is detailed in [2]. *Sonnet* and *ADS* simulations are in good agreement with the measured results.

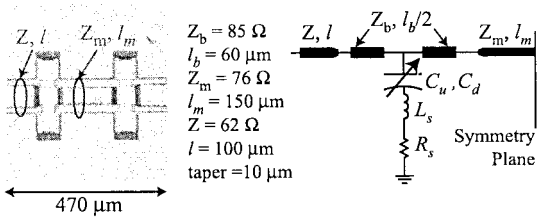


Fig. 3. π-circuit with CPW shunt capacitive MEMS switches, and its equivalent circuit.

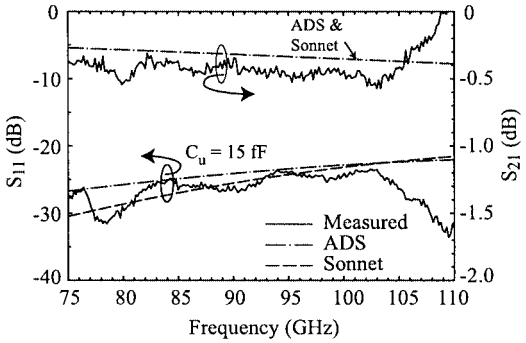
B. π-Match Design

The isolation of the W-band CPW capacitive MEMS switch can be further improved using a π-circuit design [3] (Fig. 3). Fig. 4(a) presents the measured results of a π-design in the up-state position. The high-impedance line between the bridges has G/W/G = 30/60/30 μm ($Z_m = 76\ \Omega$) and is 150-μm long, and the reference planes are 470 μm apart. A return loss better than −25 dB is obtained over the entire W-band region and the insertion loss is around −0.4 dB. The fitted up-state capacitance using *ADS* is $C_u = 15 \pm 1$ fF and is consistent with the values found for the T-match design. The simulated insertion loss by *ADS* and *Sonnet* agrees well with the measured value of −0.4 dB at 90 GHz.

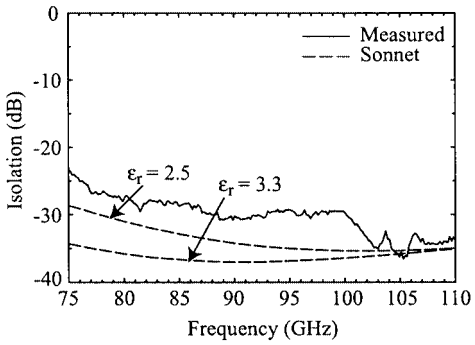
Fig. 4(b) shows the measured isolation of the π-match design in the down-state position. The isolation is better than −25 dB over the entire W-band region and is better than −30 dB above 85 GHz. Full-wave *Sonnet* simulations with a dielectric interlayer of $\epsilon_r = 2.5$ fits the measured isolation well. This is equivalent to a down-state capacitance of 300 fF. By increasing the

[1]*Advanced Design System 2002*, Agilent Technol., Santa Clara, CA, 2002.

[2]*Sonnet EM Suite*, rel. 6.0a, Sonnet Software Inc., Liverpool, NY, 1998.



(a)



(b)

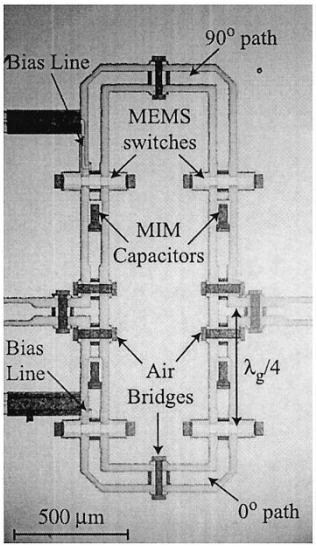
Fig. 4. Measured S-parameters of a π-match switch: (a) in the up-state position and (b) in the down-state position.

capacitance to 400 fF ($\epsilon_r = 3.3$), the isolation increases a little bit more and does not fit the measured results as well. An *ADS* model with $C_d = 400$ fF, $L_s = 5$ pH, and $R_s = 1\ \Omega$ predicts a much higher isolation (≤ -40 dB) and does not agree with the measurements. The isolation is limited to -30 dB due to electromagnetic coupling in the substrate, as predicted by the full-wave analysis.

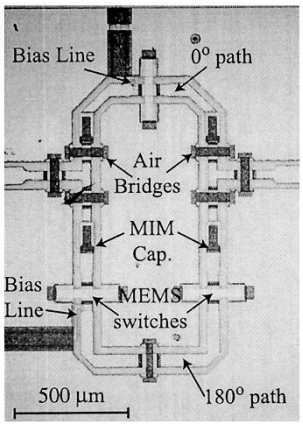
III. W-Band 1-bit Phase Shifters

Many MEMS phase shifters have been developed over the last 3–4 years [13]–[18], but little work has been done at W-band frequencies. The only MEMS W-band phase shifter developed thus far is an analog distributed MEMS transmission line by Barker and Rebeiz [14]. It exhibits -5 dB of loss for 360° of phase shift and the 0° state has an insertion loss around -2.5 dB. On the other hand, W-band monolithic microwave integrated circuit (MMIC) GaAs phase shifters were developed several years ago by Weinreb *et al.* [21] (analog design) and Zuefle *et al.* [22] (digital design). For the analog GaAs phase shifter, the insertion loss varied from -6.2 to -11.2 dB (phase shift from 0° to 358°) at 94 GHz. The 4-bit high electron-mobility transistor (HEMT) phase shifters resulted in an insertion loss of -12.5 ± 2.5 dB (3.1 dB/bit).

This section discusses the design and measurements of W-band switched-line MEMS digital phase shifters on quartz substrates. The phase shifters switch between 0°–90° or 0°–180°. Cascading the 1-bit phase shifters results in a 2-bit phase shifter with 0°/90°/180°/270° states. The advantage of the switched-line phase shifter is that it can cover a wide bandwidth with good phase-shift linearity.



(a)



(b)

Fig. 5. CPW W-band switched-line phase shifters. (a) 0°/90° phase shift (1.3×2.3 mm^2) and (b) 0°/180° phase shift (1.3×1.85 mm^2).

A. Design

Fig. 5(a) presents the fabricated 1-bit 0°/90° phase shifter with a total area of 1.3×2.3 mm^2. The three bridges at each T-junction are 140-μm long and are used for ground-plane equalization and to suppress slot modes. The MEMS bridges are placed $\lambda_g/4$ away from the T-junctions and when the upper (or lower) MEMS bridges are pulled down, they create an open circuit at the T-junction, and the millimeter-wave signal will only pass through the lower (or upper) path. The difference in line length between the two arms is 90° at 90 GHz. At each side of the T-junction, series metal–insulator–metal (MIM) capacitances are placed to block the dc-bias voltage from actuating the MEMS bridges in the opposite arm. The MIM dimensions are $40 \times 80\ \mu$m^2 and the Si_3N_4 dielectric layer is 1500-Å thick with a relative dielectric constant $\epsilon_r = 7.6$ resulting in a MIM capacitance of 1.45 pF ($X = -j1.2\ \Omega$ at 90 GHz).

The line dimensions used in both paths are $\mathrm{G/W/G} = 30/60/30\ \mu$m resulting in a characteristic impedance of 75 Ω. This impedance is chosen since it has the lowest t-line loss (Fig. 6). The values are calculated using *ADS-LineCalc*

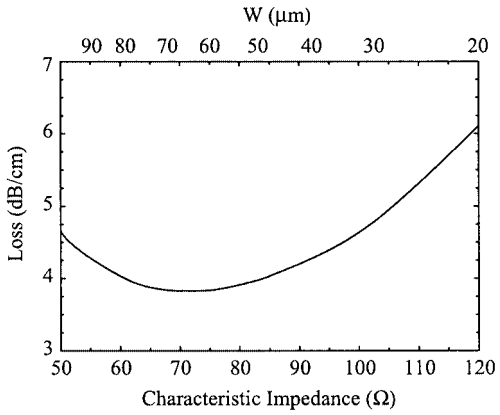


Fig. 6. Simulated loss (in decibels per centimeter) at 90 GHz for CPW lines as a function of line characteristic impedance for $\mathrm{W} + 2\mathrm{G} = 120\ \mu$m.

by varying the center conductor width, but leaving the ground-to-ground spacing fixed to 120 μm. This value is chosen in order to keep the $\mathrm{W} + 2\mathrm{G} \leq \lambda_{\mathrm{d}}/10$ (140 μm) at 110 GHz. The losses are normalized to the measured loss of 4 dB/cm by the thru-reflect line (TRL) calibration for a 62-Ω line ($\mathrm{G/W/G} = 20/80/20\ \mu$m). The t-line underneath each MEMS bridge is tapered to $\mathrm{G/W/G} = 35/50/35\ \mu$m (83 Ω) to reduce the up-state capacitance of the bridge, as presented above.

In fact, the phase-shifter design is quite involved and careful design is needed in order to get good performance. One of the major problems is that the simulation software that predicts the behavior of the individual MEMS switches (i.e. *Sonnet*) has intrinsic problems when simulating large electromagnetic circuits. The problems stem from the fact that *Sonnet* needs to include the circuit in a metal box for accurate simulations and this box creates modes which interfere and mask the real S-parameters response of the circuit. Therefore, many different simulations have been conducted in order to optimize the design (and deembed the real performance from the parasitic box modes) and this approach was quite successful, as seen below in the measured results.

Fig. 5(b) shows the 0°/180° phase shifter with dimensions 1.3×1.85 mm^2. In this case, one bridge is used in the 0° path and it is $\lambda_g/4$ away from both T-junctions. The difference in the two paths lengths is 180° at 90 GHz. The circuit is very similar to the 0°/90° phase shifter and the design approach is the same.

B. Measurements

The measured performances of both 0°/90° and 0°/180° phase shifters are shown in Fig. 7. The return loss is better than −10 dB from 75–100 GHz with an average insertion loss of −1.75 dB at 75–97 GHz. The breakdown of the insertion loss is given in Table I, and the phase shifts for both circuits are given in Fig. 7(c). The measured phases have excellent linearity with values of 99° and 202° at 90 GHz. These phase shifts are higher than the targeted values of 90° and 180° at 90 GHz due to the simulation problems stated in Section III-A.

The loss of a single MEMS switch including the matching network has been presented before and is −0.2 dB (reference planes are 380 μm apart, see Fig. 1). Also, the loss of a single air-bridge can be estimated to be −0.1 dB (reference planes are 200 μm apart). When the MEMS bridge is in the down-state position, the $\lambda_g/4$ open circuit at the T-junction results in a −0.1 dB of loss due to the many reflections the signal experiences before going through the correct path.

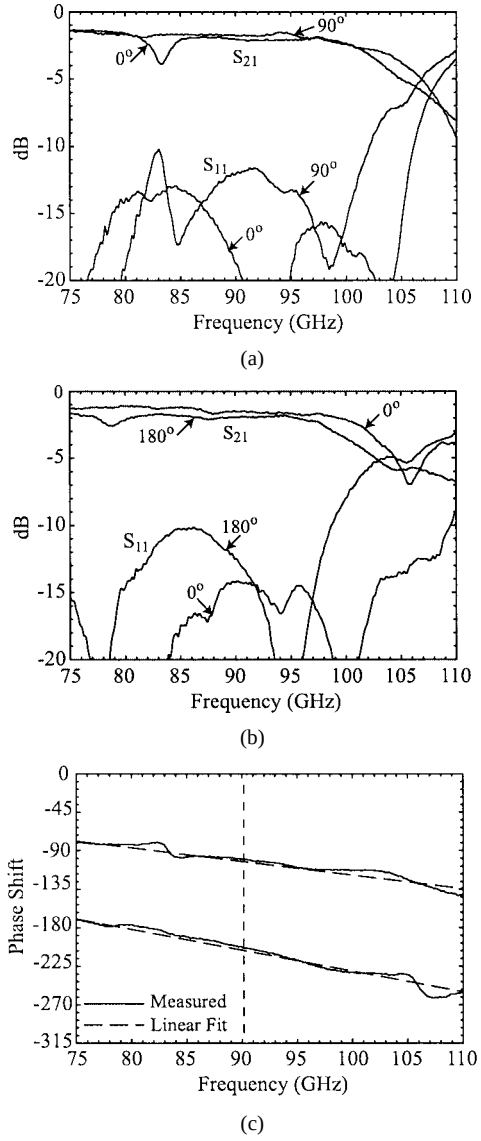


Fig. 7. CPW W-band switched-line phase shifters measured performance for both designs in both states. S-parameters for the: (a) 0°/90° and (b) 0°/180° phase shifters. (c) Phase shift in degrees.

TABLE I
BREAKDOWN OF THE CPW PHASE-SHIFTER LOSSES FOR THE 0°/90° AND THE 0°/180° PHASE SHIFTERS

Component (dB)	90° network	180° network
Av. Return Loss (1-$\lvert S_{11}\rvert^2$)	-0.15	-0.15
Switch Loss (up-state)	-0.4	-0.2 & -0.4
Switch Loss (down-state)	-0.2	-0.2
Air Bridge Loss	-0.5	-0.4 &-0.5
Remaining Line Loss	-0.4 & -0.6	-0.3 & -0.4
Bias Line Loss	-0.15	-0.15
Total Simulated	-1.8 & -2.0	-1.4 & -1.8
Total Measured	-1.85 ± 0.35	-1.65 ± 0.35

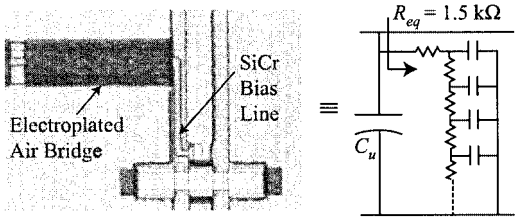


Fig. 8. Equivalent-circuit model of the biasing scheme of the CPW MEMS bridges.

The additional line loss is estimated by multiplying the remaining line length of the phase shifter by the extrapolated line loss for a 75-Ω line (3.8 dB/cm at 90 GHz, measured from the TRL calibration). The 0°/90° phase shifter has a total line length of 2800 and 3400 μm for the 0° and 90° states, resulting in a loss of -0.4 and -0.6 dB when the line lengths associated with the bridges are deducted. The 0°/180° phase shifter has a total line length of 2000 and 2800 μm for the 0° and 90° states, resulting in an additional line loss of -0.3 and -0.4 dB, respectively.

For the MIM capacitors, their effect on the line loss is negligible for a Q of ten. The loss attributed to the MIM capacitor is due to its series resistance, and the value of this series resistance is calculated using

$$Q = \frac{1}{\omega C_{\mathrm{MIM}} R_s}. \tag{4}$$

For an estimated $Q = 10$ at 90 GHz and $C_{\mathrm{MIM}} = 1.45$ pF, the series resistance is $R_s = 0.12\ \Omega$ and the insertion loss associated with this series resistance is -0.01 dB, which can be easily neglected.

On the other hand, the influence of the bias line on the insertion loss is more important. In fact, the bias line couples to the ground plane (Fig. 8) and, therefore, the CPW center conductor "sees" a relatively smaller resistance to ground (around 1500 Ω simulated using *Sonnet*) than the total dc bias line resistance (10–20 kΩ). The insertion loss due to the bias line resistance coupling to ground is given by

$$\mathrm{Loss} = 10\log_{10}\left(\frac{\mathrm{R_{eq}}}{\mathrm{Z_o} + \mathrm{R_{eq}}}\right). \tag{5}$$

Therefore, considering $R_{\mathrm{eq}} = 1500\ \Omega$, the corresponding insertion loss is -0.15 dB. Table I shows that the phase-shifter loss can be accurately predicted and that it is hard to achieve 1.4–1.5 dB/bit at W-band frequencies for 90° and 180° delays using CPW lines. Cascading the two designs together will result in a 2-bit phase shifter with a simulated average loss of -3.5 dB at 90 GHz.

IV. Conclusion

W-band low-loss and high-isolation capacitive MEMS switches have been presented in a CPW configuration on quartz substrates. The measurements have indicated a very low loss and a high isolation response over the entire W-band frequency range. MEMS switches have been used to implement very low-loss (1.75 dB/bit) switched-line phase shifters over a wide bandwidth. To our knowledge, this is the lowest reported loss/bit for any phase shifter at W-band frequencies.

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Prof. Rebeiz was the recipient of the 1991 National Science Foundation Presidential Young Investigator Award and the 1993 URSI International Isaac Koga Gold Medal Award. He was selected by his students as the 1997–1998 Eta Kappa Nu EECS Professor of the Year. In October 1998, he was the recipient of the Amoco Foundation Teaching Award, given yearly to one faculty member of The University of Michigan at Ann Arbor for excellence in undergraduate teaching. He was the corecipient of the IEEE 2000 Microwave Prize. In 2003, he was the recipient of the Outstanding Young Engineer Award of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) and a Distinguished Lecturer for the IEEE MTT-S.